WHAT IS CLAIMED IS:

1. A phase-locked loop within an integrated circuit assembly, the phase-locked loop comprising:

a plurality of subcells of semiconductor devices arranged in a base layer pattern on base layers of the integrated circuit assembly; and

one or more metal layers formed over and interconnecting the plurality of semiconductor devices in a metallization pattern, wherein the phase-locked loop has an output frequency range that is changeable with a change to the metallization pattern without a corresponding change to the base layer pattern.

2. The phase-locked loop of claim 1 wherein the plurality of subcells comprises a plurality of voltage-controlled oscillator (VCO) subcells, wherein each VCO subcell has a different oscillating frequency range, and wherein the metallization pattern operatively couples one of the VCO subcells into the phase-locked loop and operatively decouples the other VCO subcells from the phase-locked loop.

3. The phase-locked loop of claim 1 wherein the plurality of subcells comprises a loop filter subcell, which comprises a plurality of loop filter capacitors and wherein the metallization pattern

operatively couples a selected number of the loop filter capacitors into the phase-locked loop and operatively decouples any remaining ones of the loop filter capacitors out of the phase-locked loop such that the loop filter has an effective capacitance that is selectable with the metallization pattern.

4. The phase-locked loop of claim 1 wherein the plurality of subcells comprises a clock buffer subcell, which drives a clock output from the phase-locked loop, wherein the clock buffer subcell comprises a plurality of clock buffer circuit configurations, which are selectable with the metallization pattern.

5. The phase-locked loop of claim 4 wherein, for each of the clock buffer configurations, the metallization pattern operatively couples a first subset of the semiconductor devices in the clock buffer subcell to implement a corresponding clock buffer function and operatively decouples a second, different subset of the semiconductor devices in the clock buffer subcell.

6. The phase-locked loop of claim 5 wherein the clock buffer function comprises a frequency divider having a divisor that is selectable with the metallization pattern.

7. The phase-locked loop of claim 5 wherein the clock buffer function comprises a voltage level shifter having an output drive power and an output switching speed that are selectable with the metallization pattern.

8. The phase-locked loop of claim 1 wherein the plurality of subcells comprises:

a voltage-controlled oscillator subcell;

a voltage regulator subcell, which biases the voltage-controlled oscillator subcell and comprises a plurality of voltage regulator circuit configurations, which are selectable with the metallization pattern, wherein for each of the voltage regulator circuit configurations, the metallization pattern operatively couples a first subset of the semiconductor devices in the voltage regulator subcell and operatively decouples a second, different subset of the semiconductor devices.

9. A phase-locked loop (PLL) cell for fabrication on an integrated circuit, the cell definition comprising:

a first PLL configuration formed by a first plurality of subcells, wherein each of the first plurality of subcells comprises a

base layer pattern and a metallization pattern; and

a second PLL configuration formed by a second plurality of subcells, wherein at least one of the second plurality of subcells is common with a corresponding one of the first plurality of subcells and has the same base layer pattern and the same metallization pattern and wherein at least another one of the second plurality of subcells is common with a corresponding one of the first plurality of subcells and has the same base layer pattern and a different metallization pattern.

10. The PLL cell of claim 9 wherein the second plurality of subcells further comprises at least one subcell that has a different base layer pattern and a different metallization pattern than a corresponding one of the first plurality of subcells.

11. The PLL cell of claim 9 wherein the phase-locked loop comprises a phase-frequency detector subcell, which is common to the first plurality of subcells and the second plurality of subcells and has the same base layer pattern and metallization pattern in the first and second PLL configurations.

12. The PLL cell of claim 9 wherein the phase-locked loop comprises a charge pump subcell, which is common to the first plurality of subcells and the second plurality of subcells and has the same base layer pattern and metallization pattern in the first and second PLL configurations.

13. The PLL cell of claim 9 wherein the first plurality of subcells comprises a first voltage-controlled oscillator subcell and the second plurality of subcells comprises a second voltage-controlled oscillator subcell, which has a different base layer pattern and a different metallization pattern than the first voltage-controlled oscillator subcell.

14. The PLL cell of claim 9 wherein the phase-locked loop comprises a loop filter subcell, which is common to the first plurality of subcells and the second plurality of subcells and comprises a plurality of loop filter capacitors, wherein the loop filter subcell has a first metallization pattern in the first PLL configuration and a second, different metallization pattern metallization pattern in the second PLL configuration, and wherein the first and second metallization patterns operatively couple respective numbers of the loop filter capacitors into the phase-locked loop and operatively decouple remaining ones of the loop filter capacitors out of

the phase-locked loop such that the loop filter subcell has an effective capacitance that is selectable with the first and second metallization patterns.

15. The PLL cell of claim 9 wherein the phase-locked loop comprises:

a voltage-controlled oscillator subcell; and

a voltage regulator subcell, which is common to the first plurality of subcells and the second plurality of subcells and has the same base layer pattern and different metallization patterns in the first and second PLL configurations, wherein the metallization pattern in the first PLL configuration operatively couples a first set of semiconductor devices in the base layer pattern into the voltage regulator subcell and the metallization pattern in the second PLL configuration operatively couples a second, different set of semiconductor devices in the base layer pattern into the voltage regulator subcell.

16. The PLL cell of claim 9 wherein the phase-locked loop comprises a clock buffer subcell which is common to the first plurality of subcells and the second plurality of subcells and has the same base layer pattern and different metallization patterns in the

first and second PLL configurations, wherein the metallization pattern in the first PLL configuration operatively couples a first set of semiconductor devices in the base layer pattern into the clock buffer subcell and the metallization pattern in the second PLL configuration operatively couples a second, different set of semiconductor devices in the base layer pattern into the clock buffer subcell.